Anirudh S Iyengar

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SoC Design Engineer with an **end-to-end** experience from architecture/micro-architecture design, RTL/Logic design, to timing and Floor-planning around the ARM ecosystem, looking to pursue a career in **SoC architecture and design**.

Technical Skills

- **FE:** Verilog & System Verilog HDL, Spyglass LINT & CDC, Fishtail timing Constraint, VCLP-UPF, Magillem for IPXACT & Reg bank generation, memory-macro generation via memory compiler.
- **IP Config tools:** CoreConsultant, Arteris Flex NoC
- **Simulation:** Zero-delay and GLS simulation analysis on Verdi
- **PD:** Exposure to Fusion Compiler, RTLA
- **CKT/Logic Sim:** Matlab, LT-Spice, Hspice, Model SIM, Questa SIM

Education

Pennsylvania State University — Aug 2018
Doctor of Philosophy (Ph.D.) in Electrical Engineering & Computer Science.

University of South Florida — May 2013
Master of Science in Electrical Engineering (M.S.E.E).

Manipal Institute of Technology — June 2010
Bachelor of Engineering (B.E.) in Instrumentation and control

Professional Experience

SoC Design Engineer, Programmable Solutions Group (PSG) Intel Corp. — **Jan 2020-present**

- **Partition owner for the Application Processor and Micro-processor unit (ARM processor cluster) sub-system for Agilex-5 Hard Processor Subsystem.**
  - → Full partition design ownership entailed:
    - Working with architects in triaging and translating Landing Zone requirements.
    - Defining the microarchitecture (logic, timing and power)
    - RTL integration into a full chip SoC or discrete component design
    - Working with IP providers to integrate and validate IPs at the SoC level. Drove quality assurance compliance for smooth IP SoC handoff.
    - Performing quality checks in various logic design aspects ranging from RTL to timing and power convergence.
    - Working with DFX teams towards integrating MBIST and Test Control flows.
    - Applying various strategies, tools, and methods to write RTL and optimize logic to qualify the design to meet power, performance, area, and timing goals as well as design integrity and floorplanning for physical implementation.
    - Reviewing the verification plan and implementation to ensure design features are verified correctly and resolves and implements corrective measures for failing RTL tests to ensure correctness of features.
    - Following secure development practices to address the security threat model and security objects within the design coverage
    - Working with SW and Post-Si teams to drive coverage and quality.
    - Post-Si debug efforts across various teams and disciplines.

- **Partition owner for the Micro-processor unit (ARM processor cluster) sub-system for next-gen Agilex Family of products**

  → Full partition design ownership:

  - Tech Readiness efforts with architects in triaging and translating Landing Zone requirements.
  - Defining the microarchitecture (logic, timing and power)
  - RTL integration into a full chip SoC or discrete component design
  - Working with IP providers to integrate and validate IPs at the SoC level. Drove quality assurance compliance for smooth IP SoC handoff.
  - Applying various strategies, tools, and methods to write RTL and optimize logic to qualify the design to meet power, performance, area, and timing goals as well as design integrity and floor-planning for physical implementation.
  - Translating the micro-architecture behind Dynamic Voltage and Frequency scaling and Dynamic Power Gating of the ARM cores (involving PD analysis).

- **Helped qualify and sign-off the FE collateral for Intel eASIC N5X Hard Processor Subsystem.**

Security Researcher, Intel Product Assurance and Security (IPAS) Intel Corp. **Jul 2018-Dec 2019**

- Analyzing and evaluating security concerns surrounding the Intel server platform.
- Researching upcoming threats that can compromise Intel products.
- SHA-512/384/256 for Security Device Manager (SDM): Worked with Intel Labs in designing and optimizing the SHA implementation for the SDM around area and delay.

Student Intern at Security Center of Excellence (SeCoE) Intel Corp. **Summer 2017**

- Worked on a security validation framework/tool for writing tests centered on IP security validation.

Student Intern at Security Center of Excellence (SeCoE) Intel Corp. **Summer 2016**

- Worked on realizing the 3DXpoint memory as a Physically Unclonnable Function (PUF).

Journal Publications

- **A. Iyengar**, S. Ghosh, K. Ramclam, "Domain Wall Magnets for Embedded Memory and Hardware Security"**, JETCAS**, 2014.
- S. Motaman, **Anirudh Iyengar**, and S. Ghosh, “Domain Wall Memory—layout, circuits and synergistic systems”, **TNANO**, 2014. **Impact Factor: 1.62.**
- **A. Iyengar**, S. Ghosh, and J. Jang. "MTJ-Based State Retentive Flip-Flop with Enhanced-Scan Capability to Sustain Sudden Power Failure." **TCAS-I** (2015).
- **A. Iyengar**, S. Ghosh, K. Ramclam, J. Jang and C. Lin, "Spintronic PUFs for Security, Trust and Authentication" **JETC** (Special Issue on Secure and Trustworthy Computing), 2015.
- **A. Iyengar**, S. Srinivasan and S. Ghosh, “Retention Testing Methodology for STTRAM” **IEEE Design & Test**, 2016.
- S. Ghosh, **A. Iyengar** et. al, “Circuits, Systems and Applications of Spintronics” **JETCAS**, 2017.
- S. Ghosh, RV Joshi, D Somasekhar, X Li, **A. Iyengar** et. al, "EMERGING MEMORIES—TECHNOLOGY, ARCHITECTURE, AND APPLICATIONS—SECOND ISSUE" **JETCAS,** 2017**.**
- S. Ghosh, R. Jha, **A. Iyengar,** and R. Govindaraj. "Design Space Exploration for Selector Diode-STTRAM Crossbar Arrays." IEEE Transactions on Magnetics **(TMAG)** 54, no. 6 (2018): 1-5.
- **A. Iyengar**, S. Ghosh, & N. Rathi, (2018). Magnetic Tunnel Junction Reliability Assessment under Process Variations and Activity Factors and Mitigation Techniques. Journal of Low Power Electronics **(JOLPE)**, 14(2), 217-226.
- N. I. Khan, **A. Iyengar** & S. Ghosh “Novel Magnetic Burn-In for Retention and Magnetic Tolerance Testing of STTRAM” IEEE Transactions on Very Large Scale Integration (VLSI) Systems **(TVLSI),** 2018**.**
- JW. Jang, A. De, D. Vontela, I. Nirmala, S. Ghosh **& A. Iyengar**, S. Ghosh, “Threshold-defined Logic and Interconnect for Protection against Reverse Engineering” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), 2018.

Conference Paper Publications

- **A. Iyengar** and S. Ghosh, “Modeling and analysis of domain wall dynamics for robust and low-power embedded memory.” In Design Automation Conference **(DAC)**, 2014 51st ACM/EDAC/IEEE, pp. 1-6. IEEE, 2014.
- **A. Iyengar,** K. Ramclam, S. Ghosh, "DWM-PUF: A Low-overhead, Memory-based Security Primitive." In Hardware-Oriented Security and Trust **(HOST)**, 2014 IEEE International Symposium on, pp. 154-159. IEEE, 2014.
- S. Motaman, **A. Iyengar**, and S. Ghosh. "Synergistic circuit and system design for energy-efficient and robust domain wall caches." In Proceedings of the 2014 international symposium on Low power electronics and design **(ISLPED)**, pp. 195-200. ACM, 2014.
- N. Rathi, S. Ghosh, **A. Iyengar** and H. Naeimi, “Data Privacy in Non-Volatile Cache: Challenges, Attack Models and Solutions.” In Design Automation Conference **(ASP-DAC),** 2016 21st Asia and South Pacific, pp. 348-353. IEEE, 2016.
- **A. Iyengar** and S. Ghosh, “Threshold Voltage-Defined Switches for Programmable Gates”, **GOMACTech**, 2015.
- I. Nirmala, D. Vontela, S. Ghosh, **A. Iyengar** “A novel threshold voltage defined switch for circuit camouflaging.” In Test Symposium **(ETS),** 2016 21th IEEE European, pp. 1-2. IEEE, 2016.
- **A. Iyengar,** “Retention Testing Methodology for STTRAM” **TECHCON 2016**.
- **A. Iyengar,** S. Ghosh, N. Rathi & H. Naeimi "Side channel attacks on STTRAM and low-overhead countermeasures." In 2016 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems **(DFT),** pp. 141-146. IEEE, 2016**.**
- **A. Iyengar,** N. Vobilisetti & S. Ghosh, “Authentication of Printed Circuit Boards.” In 42nd International Symposium for Testing and Failure Analysis, (**ISTFA)** 2016. ASM International, 2016.
- N.I.Khan, **A. Iyengar** & S. Ghosh “Novel Magnetic Burn-In for Retention Testing of STTRAM.” In 2017 Design, Automation & Test in Europe Conference & Exhibition **(DATE**). IEEE, 2017**.**
- A. De, **A. Iyengar** et. al, “CTCG: Charge-Trap Based Camouflaged Gates for Reverse Engineering Prevention.” In 2018 IEEE International Symposium on Hardware Oriented Security and Trust **(HOST)**, pp. 103-110. IEEE, 2018.
- **A. Iyengar,** et. al “Threshold Defined Camouflaged Gates in 65nm Technology for Reverse Engineering Protection.” In Proceedings of the International Symposium on Low Power Electronics and Design (**ISLPED)**, p. 6. ACM, 2018.

Posters

- **A. Iyengar**, K. Ramclam, Jae-Won Jang & C. W. Lin, “Spintronic PUFs for Security, Trust and Authentication”, Cyber Security Awareness Week Conference (**CSAW**), 2014.
- **A. Iyengar**, N. Rathi, S. Ghosh, “Static and Dynamic Current Throttling for Improved Oxide Lifetime of STTRAM Arrays”, IEEE Design Automation Conference (***DAC***), 2015.
- **A. Iyengar**, S. Ghosh, D. Vontela & I. R. Nirmala “Threshold Defined Logic Engines and Applications”, Florida Institute for Cybersecurity Research (**FICS**), 2016.
- **A. Iyengar** & S. Ghosh, “Threshold Voltage-Defined Switches for Programmable Gates”, Government Microcircuit Applications & Critical Technology Conference (**GOMACTech**), 2016.
- **A. Iyengar**, F. Zhang, S. Ghosh & S. Bhunia, “Split-Manufacturing of Printed Circuit Boards”, IEEE Design Automation Conference (**DAC**), 2016.
- **A. Iyengar**, D. Vontela, I. Reddy Nirmala & S. Ghosh, “A Novel Threshold Voltage Defined Switch for Circuit Camouflaging”, IEEE European Test Symposium (**ETS**), 2016.
- **A. Iyengar,** "Spintronic memory towards Secure and Energy-Efficient Computing" **PhD Forum at DAC** 2016.
- **A. Iyengar**, “Retention Testing Methodology for STTRAM” abstract accepted for a full paper & poster presentation in **TECHCON 2016**.
- **A. Iyengar,** S. Ghosh “Side Channel Attacks on STTRAM and Low-Overhead Countermeasures” **GOMACTech 2017.**

- **A.Iyengar,** S. Ghosh “Protecting Sensitive Intellectual Property Even Under Full Reverse Engineering of Functionality” **GOMACTech 2018.**
- **A. Iyengar,** "Spintronic memory towards Secure and Low-Power Computing" **PhD Forum at DATE 2018**.

Book Chapters

- **A. Iyengar** & S. Ghosh, “Hardware Trojans and Piracy of PCBs.” In The Hardware Trojan War, pp. 125-145. Springer, Cham, 2018. Springer International.

Invention Disclosures (Patents)

- Physically unclonable function based on domain wall memory and method of use**,** Swaroop Ghosh, **Anirudh Iyengar**, and Kenneth Ramclam (US9859018B2).
- Non-Volatile Flip-Flop with Enhanced-Scan Capability to Sustain Sudden Power Failure**,** Swaroop Ghosh and **Anirudh Iyengar** (US9728241B2).
- Threshold Voltage Defined Switches for Programmable Camouflage Gates, **Anirudh Iyengar**, Swaroop Ghosh, Deepakreddy Vontela & Ithihasa Reddy Nirmala (US10177768B2)

Honors and Awards

- Received **Division Recognition Award** for my efforts in porting SM-perforce database to KM -Cheetah.
- **Won** the **Best Poster prize** at the 2018 PhD Forum at DATE.
- **Won** the **Best Poster Presentation award** at the 2016 PhD Forum at DAC.
- **Third place** in **Embedded Security Challenge** at Cyber Security Awareness Week Conference (**CSAW**), 2014.
- An article in ***IEEE XPLORE Innovation Spotlight***, titled “Domain Wall Memory: The Next Big Thing in Hardware Security?” July 2015.

References

- **Sabyasachi Dey - Sr. Director PSE FPGA Engineering**

  sabyasachi.dey@intel.com
- **Gopal Iyer - Silicon Design Engineering Manager**

  gopal.iyer@intel.com
- **Barun Paul - Silicon Domain Architect**

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- **Akash Saxena - Microarchitecture Engineer**

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